AU OPTOELECTRONICS CORPORATION

Spec. No.	

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TFT-LCD CONTROLLER LSI (UPS161)

PRELIMINARY SPECIFICATION (TENTATIVE)

MODEL NAME: UPS161

The content of this technical information is subject to change without notice. Please contact AUO or its agent for further information.

Approved by	Checked by	Prepared by

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A. General description:

This timing controller is a synchronizing signal controlling CMOS LSI for AUO COG type LCD module. It accepts 6 bits RGB digital signal and provides all the necessary control signals to the LCD source and gate drivers. This controller supports 1 channel TTL signal input for the resolution is 800x480 (WVGA) display for AUO TFT-LCD panel.

B. Feature:

*Single power supply: +3.3 Volts
*Low power consumption (CMOS)
*EMI reducing
*Flicker Auto-detecting
*DE/HV mode auto detection
*Normal /self-test mode selecting
*Built-In polarity inverted circuit
*Providing timing scan signals for Left / Right and Up / Down shift control
*With EDGSL pin to choose data latching mode (one/dual edge of clock)
*TQFP80 package

C. Pin description:

Pin-no	Symbol	I/O	Description	Remark
1	VDD	I	Power	
2	DE_OUT	O	Test pin	
3	REDUCE	I	To reduce EMI	Note1
4	GS1	I	CKV width control setting bit (MSB)	Note2
5	GS0	I	CKV width control setting bit (LSB)	
6	CR1	I	Reset pin (Low reset) – normal pull high	
7	KYESY1	I	Test pin	
8	KTEST2	I	Test pin	
9	MODE	I	Use pin “mode” to set normal (WVGA) or self-test mode. When MODE is “L”: using the CLKIN to generate the running pattern (6 patterns). When MODE is “H”: Normal condition (WVGA 800 x 480 / 60Hz).	Note3.
10	GND	-	Power ground	
11	GND	-	Power ground	
12	DCLK	I	Dot clock signal	
13	LRC	I	Normal scan set to High Reverse scan: set to Low	
14	RI0	I	Red data input (LSB)	
15	RI1	I	Red data input	
16	RI2	I	Red data input	
17	RI3	I	Red data input	
18	RI4	I	Red data input	
19	RI5	I	Red data input (MSB)	
20	GI0	I	Green data input (LSB)	
21	VDD	I	Power	
22	GI1	I	Green data input	
23	GI2	I	Green data input	
24	GI3	I	Green data input	
25	GI4	I	Green data input	
26	GI5	I	Green data input (MSB)	
27	BI0	I	Blue data input (LSB)	
28	BI1	I	Blue data input	
29	BI2	I	Blue data input	
30	BI3	I	Blue data input	
31	GND	-	Power ground	

Pin-no	Symbol	I/O	Description	Remark
32	BI4	I	Blue data input	
33	BI5	I	Blue data input (MSB)	
34	UDC	I	Normal scan or Reverse scan setting pin	Note4
35	HS	I	Horizontal synchronizing signal	
36	ENAB	I	To select DE or HV mode	Note5
37	VS	I	Vertical synchronizing signal	
38	STV1	I/O	UDC='H', STV1 is output pin of start pulse UDC='L', STV1 is input pin of start pulse	
39	STV2	I/O	UDC='H', STV2 is input pin of start pulse UDC='L', STV2 is output pin of start pulse.	
40	VDD	I	Power	
41	VDD	I	Power	
42	CKV	O	Gate-open start pulse	
43	UDO	O	Panel up/down scan control pin.	
44	OEV	O	Vertical output enable (after power on, OEV will keep high more than 2 fields)	
45	STHR	I/O	LRC='H', STHR is output pin of start pulse LRC='L', STHR is input pin of start pulse.	
46	FIELD	O	In DE MODE, controller will generator a frame signal . In HV MODE, it is VSYNC signal.	
47	EDGSL	I	"L" **à** Normal Operating, Data will be latched on the rising edge of FY "H" **à** Data will be latched on the rising edge and falling edge of FY, the FY frequency is 1/2 DCLK	
48	FY	O	"FY" Output Buffer Setting **à** 4 mA	
49	LRO	O	Panel left/right scan control pin.	
50	GND	-	Power ground	
51	GND	-	Power ground	
52	PCTR	I	Flicker Detect" Setting "L" **à** Auto Detect "Flicker Pattern" Mode 2 dot inversion (Flicker Pattern) or dot inversion(Normal display) "H" **à** Non- Flicker Pattern" detect **à** Dot inversion	
53	RO0	O	Red data output (LSB)	
54	RO1	O	Red data output	
55	RO2	O	Red data output	
56	RO3	O	Red data output	
57	VDD	I	Power	
58	RO4	O	Red data output	
59	RO5	O	Red data output (MSB)	
60	GO0	O	Green data output (LSB)	

Pin-no	Symbol	I/O	Description	Remark
61	GO1	O	Green data output	
62	GND	-	Power ground	
63	GO2	O	Green data output	
64	GO3	O	Green data output	
65	GO4	O	Green data output	
66	GO5	O	Green data output (MSB)	
67	VDD	I	Power	
68	BO0	O	Blue data output (LSB)	
69	BO1	O	Blue data output	
70	BO2	O	Blue data output	
71	BO3	O	Blue data output	
72	BO4	O	Blue data output	
73	BO5	O	Blue data output (MSB)	
74	GND	-	Power ground	
75	LD	O	Operating enable per line	
76	INV	O	Test pin	
77	POL	O	Polarity inversion signal	
78	IPOL	O	Opposed to POL signal	
79	STHL	I/O	LRC='H', STHL is input pin of start pulse. LRC='L', STHL is output pin of start pulse.	
80	VDD	I	Power	

Note1:

Use pin "Reduce" to select INV function enable or not.

à When "Reduce" is high: INV function enable.

à When "Reduce" is low: INV function disable.

INV function:

Compare nth data and n+1th data 18 bit:

If data change more than 10 bit, than

INV n+1 = /INV n, data n+1 = /(data n+1 XOR INV n)

Otherwise INV n+1 = INV n, data n+1 = data n+1 XOR INV n.

Note2. CKV pulse width setting range

GS0	GS1	Tgs
0	0	30DLCK
0	1	40DLCK
1	0	50DLCK
1	1	60DLCK

Note3. Test Pattern Generator

Generate test mode pattern and DE signal by clk (Test data and Test DE) for burn in test.

This block only enables in MODE is "L".

Timing: (800 x 480) WVGA

(2) Patterns Change :

1. White grayscale – 64 gray
2. 2.Red grayscale -- 64 gray
3. 3.Green grayscale – 64 gray
4. Blue grayscale -- 64 gray
5. White Screen
6. Black Screen
7. White Screen
8. Black Screen

Ex) 1. White gray scale
12pixel: R(5:0)=”000000”, G(5:0)=”000000”, B(5:0)=”000000”
13-24pixel: R(5:0)=”000001”, G(5:0)=”000001”, B(5:0)=”000001”
745-756pixel: R(5:0)=”111110”, G(5:0)=” 111110”, B(5:0)=” 111110”
757-768pixel : R(5:0)=”111111”, G(5:0)=” 111111”, B(5:0)=” 111111”
769-800pixel : R(5:0)=”000000”, G(5:0)=”000000”, B(5:0)=”000000”

PS1: Test Pattern
Resolution: 800x480
Horizontal blanking: 128 DCLK
Horizontal period : 928 DCLK
Vertical blanking : 45 TH
Vertical period : 525 TH

Note4. UDC setting:

For A102VW01: Normally mode – Scan direction Up to Down setting to High.
Reverse mode -- Scan direction Down to up setting to Low.

For A070VW01: Normally mode – Scan direction Up to Down setting to Low.
Reverse mode -- Scan direction Down to up setting to High.

Note5.

If ENAB signal has high/low change, ASIC will be DE mode, All of the signals will follow DE signal operating. Otherwise, ASIC will be HV mode, output signal will follow HV_ENAB signal made by HSYNC and VSYNC.

D. AC characteristics
a. Input signal characteristics

WVGA timing
(a). DE mode

Item	Symbol	Min	Typ	Max	Unit	Remark
Clock frequency	Fck	20	33.3	42	MHz	
Clock High time	Twcl	8	–	–	ns	
Clock Low time	Twch	8	–	–	ns	
Clock rising time	Trclk	–	–	1	ns	
Clock falling time	Tfclk	–	–	1	ns	
Horizontal blanking	Thbl	95	128	280	Clk	
Vertical blanking	Tvbl	32	45	184	Th	

DE setup time	Tes	5	-	-	ns	
DE hold time	Teh	10	-	-	ns	

(b). HV mode

Item	Symbol	Min	Typ	Max	Unit	Remark
Clock frequency	Fck	20	33.3	42	MHZ	
Clock High time	Twcl	8	—	—	ns	
Clock Low time	Twch	8	—	—	ns	
Clock rising time	Trclk	—	—	1	ns	
Clock falling time	Tfclk	—	—	1	ns	
Hsync period	Th	895	1056	1088	Clk	
Hsync pulse width	Thw	4	-	81	Clk	
Hsync front porch	Thf	7	40	—	Clk	
Hsync back porch	Thb	7	60	84	Clk	
Hsync width + back porch	Thw +Thb	—	88	—	Clk	
Hsync blanking	Thbl	95	128	284	Clk	
Hsync setup time	Ths	5			ns	
Hsync hold time	Thh	10			ns	
Vsync period	Tv	512	525	610	Th	
Vsync pulse width	Tvw	1	3	—	Th	
Vsync front porch	Tvf	—	13	—	Th	
Vsync blanking	Tvbl	32	45	184	Th	
Hsync/Vsync phase shift	Tvpd	2	320	—	Clk	
Vsync setup time	Tsv	0			ns	
Vsync hold time	Thv	2			ns	
Data setup time	Tds	5			ns	
Data hold time	Tdh	10			ns	

Item	Symbol	Value	Unit	Description
Horizontal display start	The	88	Clk	After falling edge of Hsync, counting 88 clk, then getting valid data from 89 th clk's data.
Vertical display start	Tve	32	Th	After falling edge of Vsync, counting 32 Th, then getting 33 th Th's data.

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
DCLK frequency	Fclk	-	33.3	-	Mhz	Vcc=2.5 ~3.6V
DCLK cycle time	Tcph	-	30	-	ns	
CLK pulse duty	Tcw	40	50	60	%	Tcph
Time that the POL transition to LD	Tpl	-	1	-	DCLK	
LD width	Tldw	-	3	-	DCLK	
Time that the CKV rising to LD	Tgs	30	-	60	DCLK	

Time that the STV1/2 rising to LD	Tgs	-	500	-	DCLK	
STV1/2 width	Tstvw	-	800	-	DCLK	
Time that the POL rising to Field	Tpf	-	1.5	-	Th	
Time that the DE rising to V_END	Tvend	-	2484	-	DCLK	

E. DC characteristics

a. Absolute maximum ratings

Symbol	Parameter	Rating	Units	Remark
V_{DD}	Power supply	2.5 to 3.6	V	
V_{IN}	Input voltage	-0.3 to VDD + 0.3	V	
VIL	Low level input voltage	GND to 0.3xVDD	V	
VIH	High level input voltage	0.7xVDD to VDD	V	
VOH	High level output voltage	VDD-0.4(minimum)	V	
VOL	Low level output voltage	GND to GND+0.4	V	
V_{OUT}	Output voltage	-0.3 to VDD + 0.3	V	
DCLK	Operating frequency	20~40	MHz	
T_{STG}	Storage temperature	-40 to 125	℃	

b. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Units	Remark
V_{DD}	Power supply	2.7	3.3	3.6	V	
IDD	Current for V	-	9.5	-	mA	
T_{OPR}	Operating temperature	-30	25	85	℃	

c. General DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IL}	Input leakage current	no pull-up or pull-down	-1	-	1	μA
I_{OZ}	Tri-state leakage current		-10	-	10	μA
C_{IN}	Input capacitance		-	3	-	pF
C_{OUT}	Output capacitance		3	-	6	pF
C_{BID}	Bi-directional buffer capacitance		3	-	6	pF

d. Current consumption for different resolution modes

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC}	I_{CC}	V_{CC1}=+3.3V	-	9.5	-	mA	

e. DC electrical characteristics for 3.3V operation

Tj= 0℃ to +65℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Remark
V_{IL}	Input Low voltage	CMOS	-	-	0.3 xV_{CC3IO}	V	
V_{IH}	Input High voltage	CMOS	0.7 x V_{CC3IO}	-	-	V	
V_{OL}	Output low voltage	I_{OL}=4mA	-	-	0.4	V	
V_{OH}	Output high voltage	I_{OH}=4mA	2.7	-	-	V	
R_I	Input pull up/down resistance	Vil=0V or Vih=V_{CC}	-	75	-	KΩ	

F. Reliability test item:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta = 125℃ 240H	
2	Low temperature storage	Ta = -40℃ 240H	
3	High temperature operation	Ta = 85℃ 240H	
4	Low temperature operation	Ta = -30℃ 240H	
5	High temperature and high humidity	Ta = 60℃ • 95%RH 240H	Operation
6	Heat shock	-30℃～+85℃/50 cycles 2H/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω),once for each terminal	Non-operation

Note : Ta is the Ambient temperature.

G. Package information

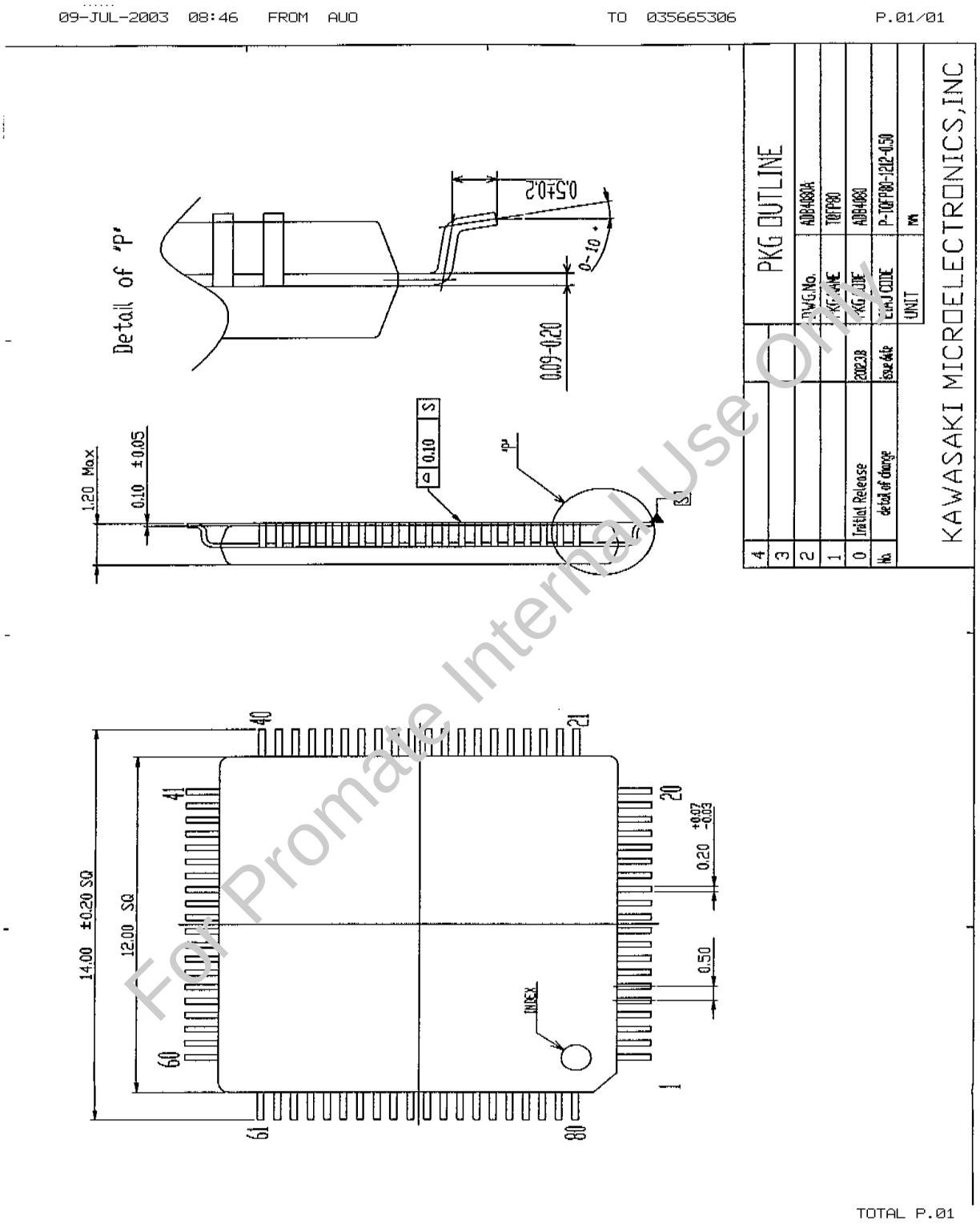
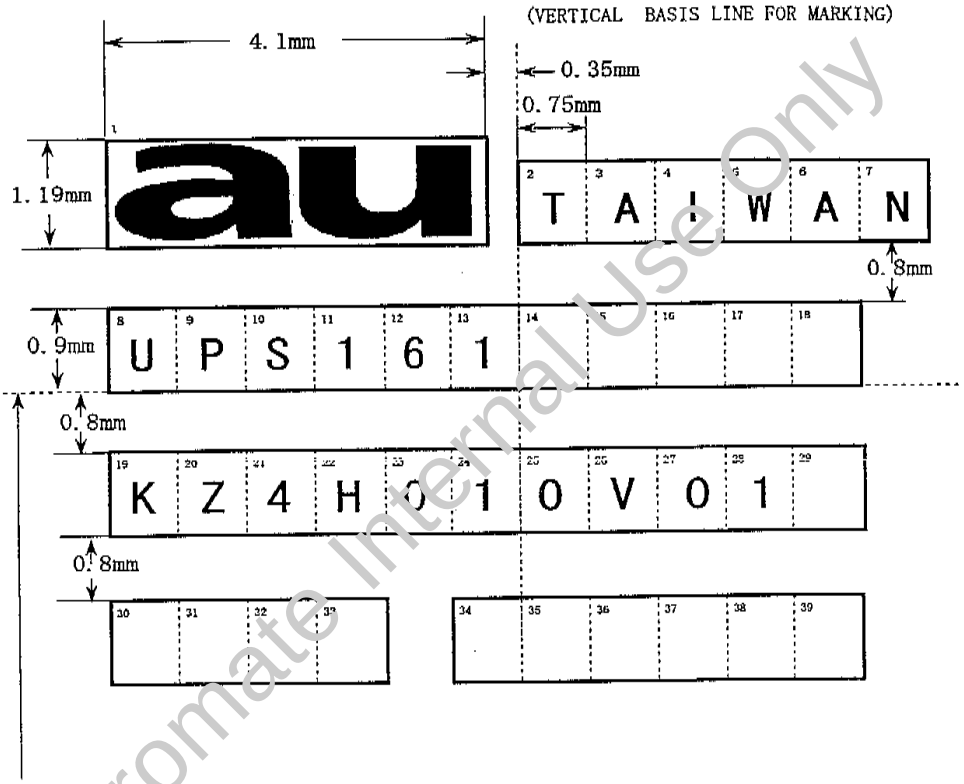


Fig1.Outline drawing

配布先

●CUSTOM MARKING DRAWINGS

PACKAGE : TQFP80 (BODY SIZE 12×12mm)
PACKAGE CODE : ADB40080
Marking : LASER



EXPLANATION OF MARK

1, 8～18 :USER'S PARTS
2～7 :MANUFACTURED COUNTRY
19～39 :KME'S PARTS

Rev.	Date	Explanation	Apr.	Che.	Pre.
0	03/02/12	新規作成			小笨

MARKING SPEC 1/1

No. KZ4H010V01 01

川崎マイクロエレクトロニクス

TOTAL P.01

Fig2. Marking spec.

Appendix

Appendix 1. Input timing diagram

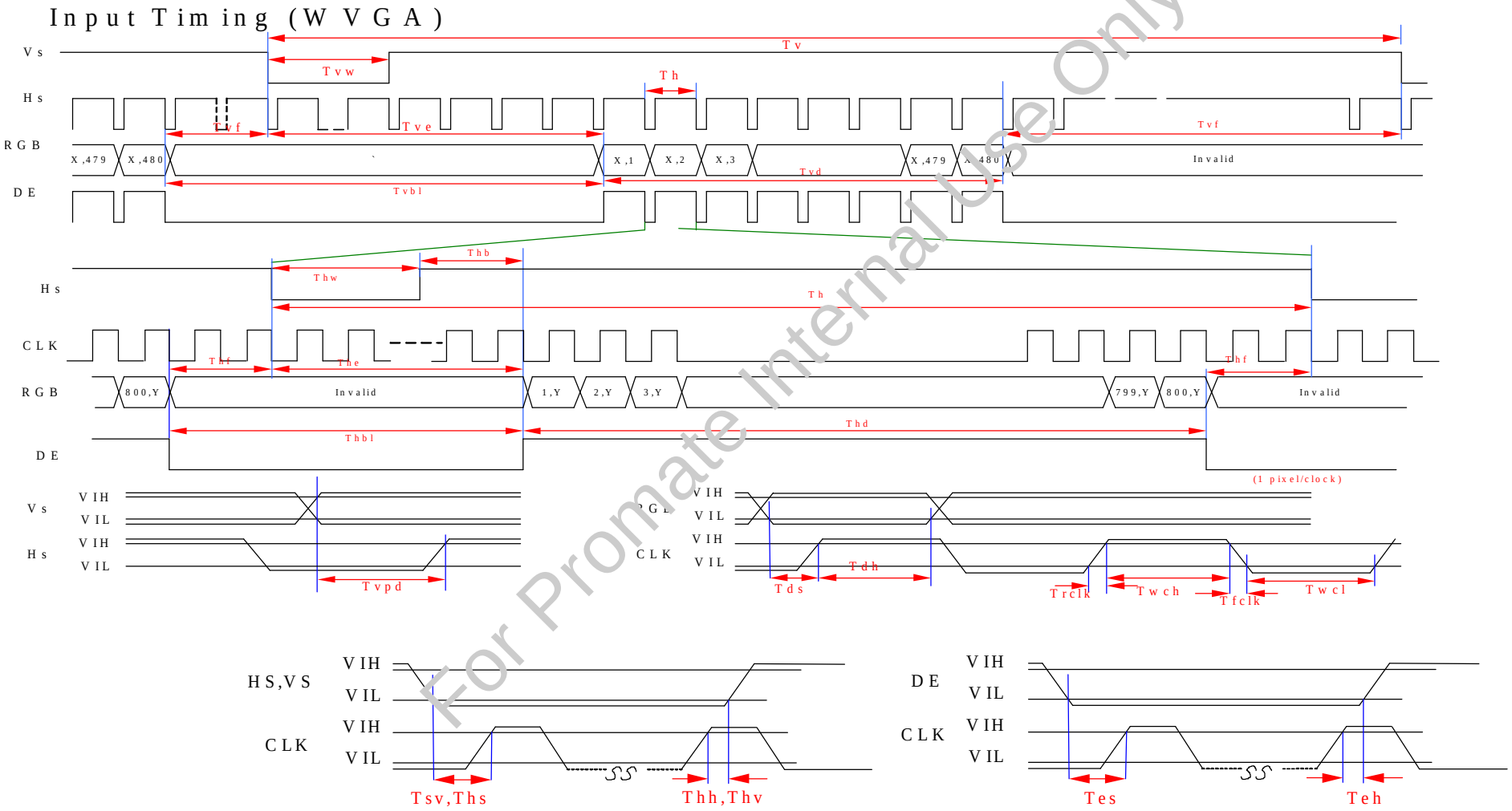
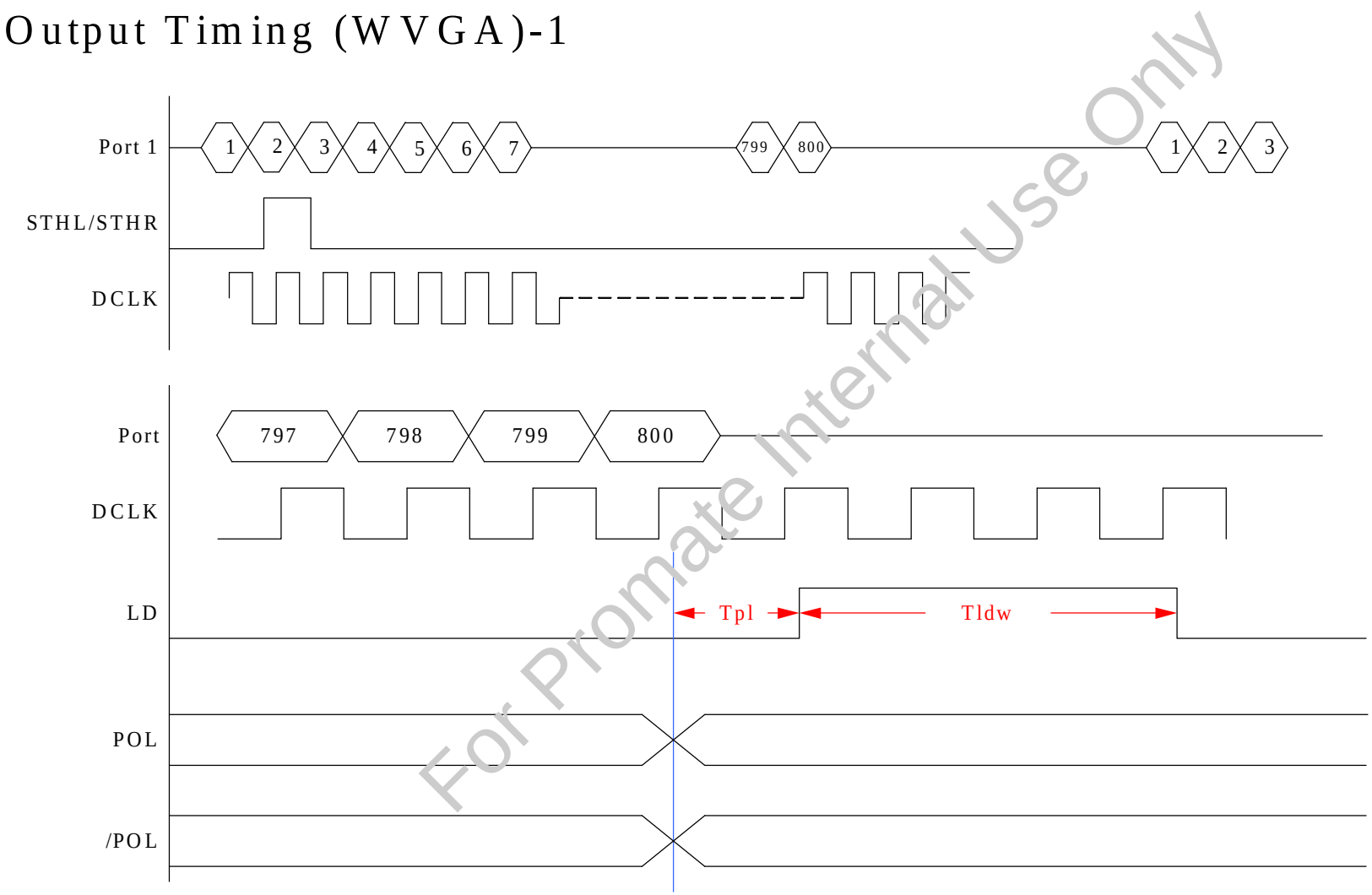
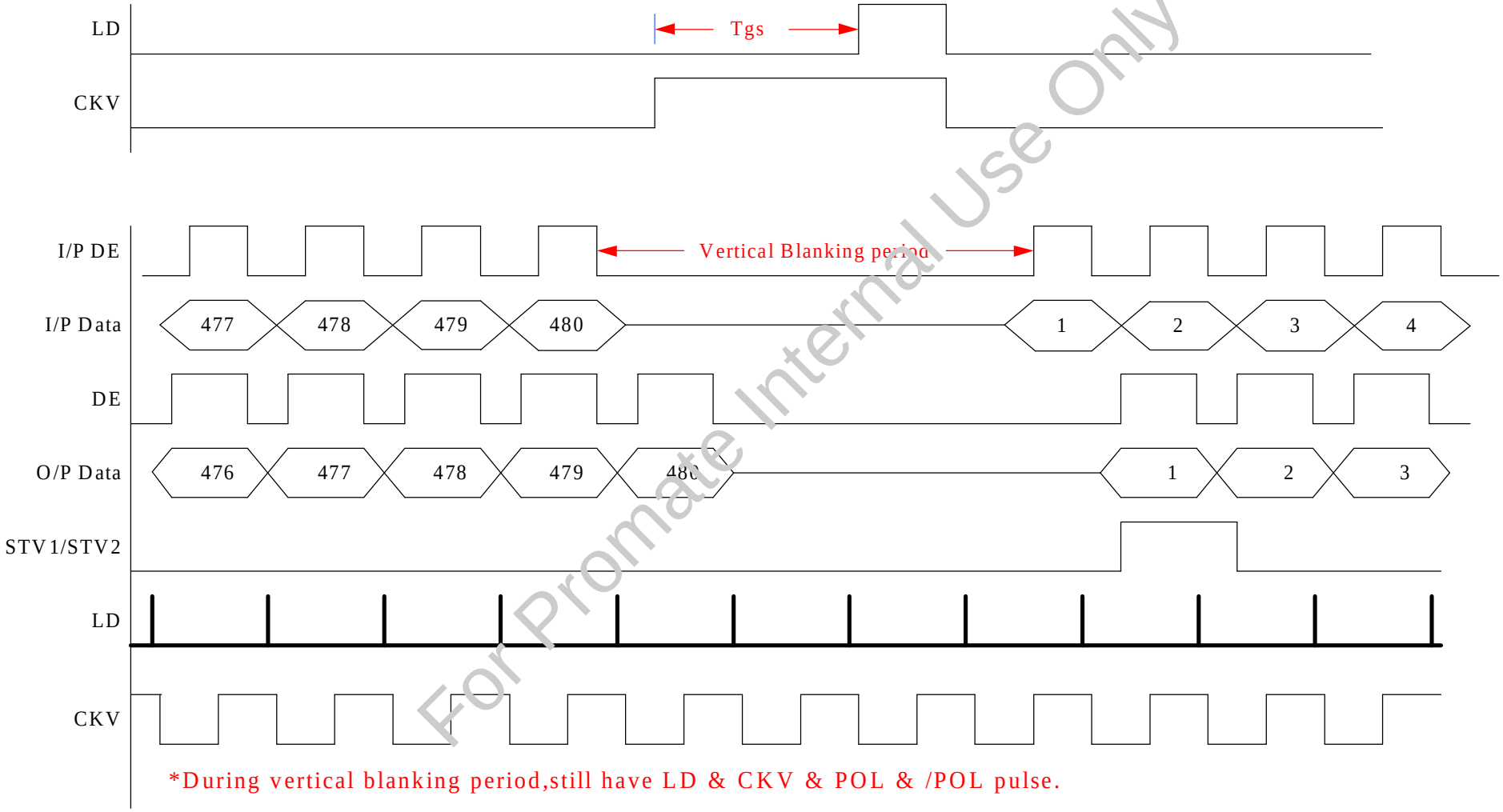


Fig3. Input timing

Appendix 2. Output timing diagram

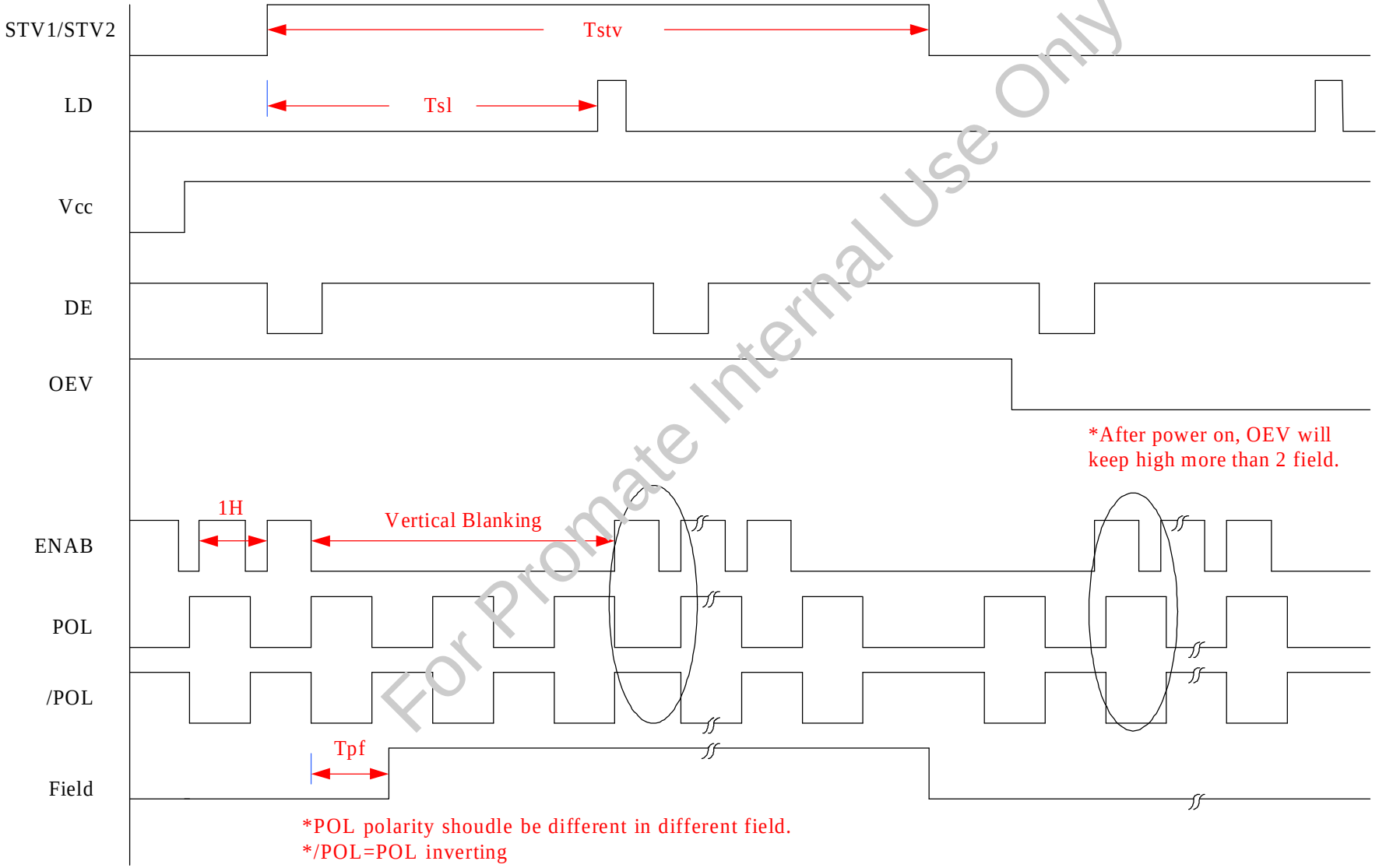


Output Timing (WVGA)-2



*During vertical blanking period,still have LD & CKV & POL & /POL pulse.

Output Timing (WVGA)-3



Output Timing (WVGA) - 4

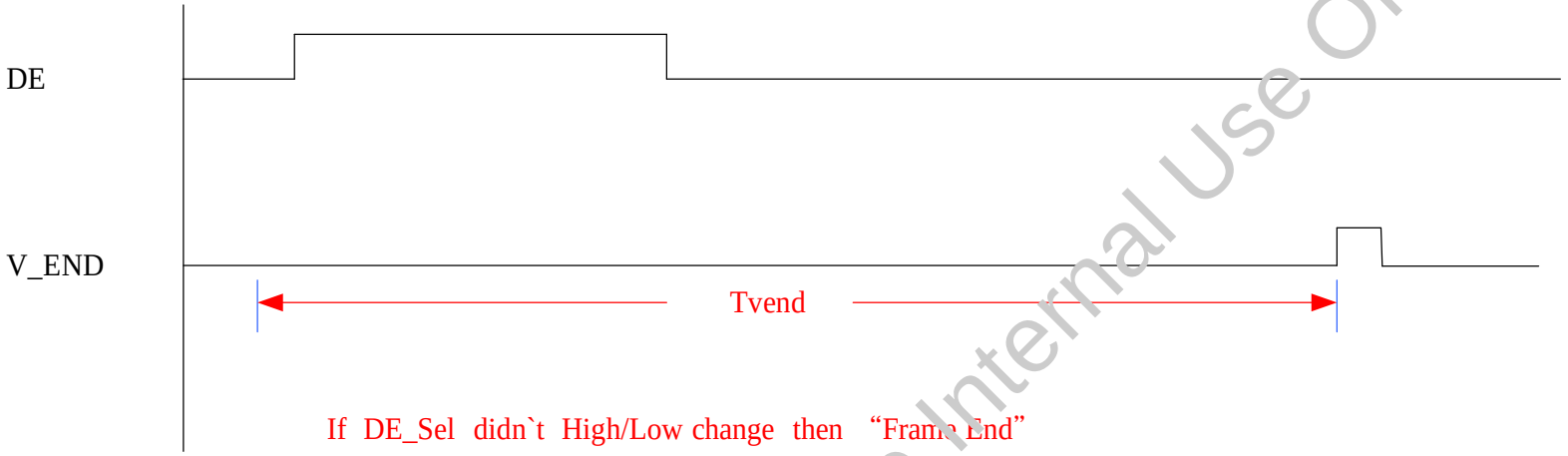


Fig4. Output timing (WVGA) 1~4

Appendix 3. EDGSL function

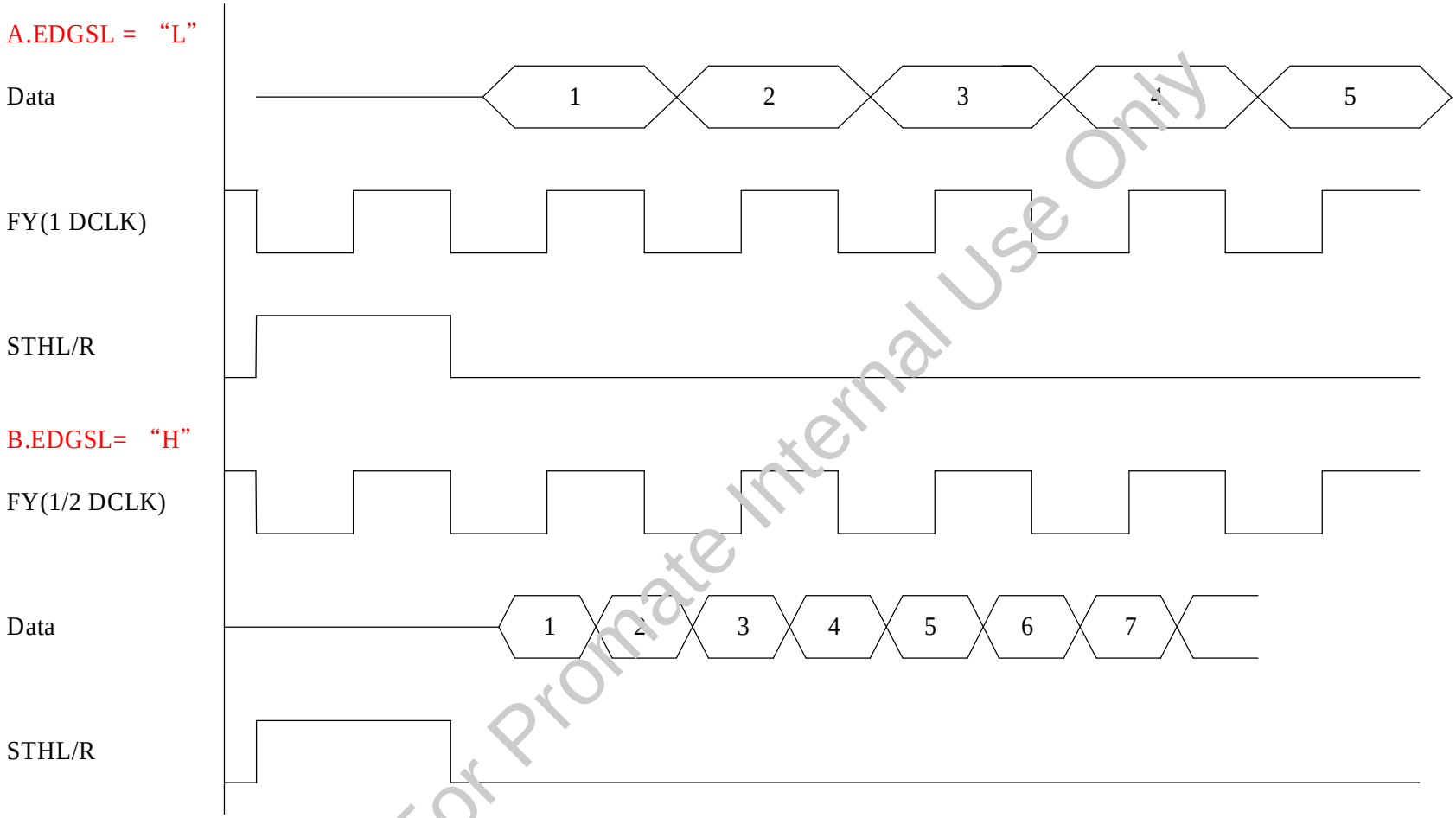


Fig5. Timing after setting EDGSL